ADNS-2620
Optical Mouse Sensor

Data Sheet

Description

The ADNS-2620 is a new entry level, small form factor optical mouse sensor. It is used to implement a non-mechanical tracking engine for computer mice. Unlike its predecessor, this new optical mouse sensor allows for more compact and affordable optical mice designs.

It is based on optical navigation technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The sensor is housed in an 8-pin staggered dual inline package (DIP). It is designed for use with the HDNS-2100 Lens, HLMP-ED80-xx000, and the HDNS-2200 LED Clip, providing an optical mouse solution that is compact and affordable. There are no moving parts, so precision optical alignment is not required, thereby facilitating high volume assembly.

The output format is a two wire serial port. The current X and Y information are available in registers accessed via the serial port.

Resolution is 400 counts per inch (cpi) with rates of motion up to 12 inches per second (ips).

Theory of Operation

The ADNS-2620 is based on Optical Navigation Technology. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP) and a two wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system provided by the HDNS-2100, HDNS-2200, and HLMP-ED80-xx000. These images are processed by the DSP to determine the direction and distance of motion.

Features

- Precise optical navigation technology
- Small form factor
  (10 mm x 12.5 mm footprint)
- No mechanical moving parts
- Complete 2D motion sensor
- Common interface for general purpose controller
- Smooth surface navigation
- Programmable frame speed up to 3000 frames per sec (fps)
- Accurate motion up to 12 ips
- 400 cpi resolution
- High reliability
- High speed motion detector
- Wave solderable
- Single 5.0 volt power supply
- Conforms to USB suspend mode specifications
- Power conservation mode during times of no movement
- Serial port registers
  – Programming
  – Data transfer
- 8-pin staggered dual inline package (DIP)

Applications

- Mice for desktop PC's, workstations, and portable PC's
- Trackballs
- Integrated input devices

Pinout of ADNS-2620 Optical Mouse Sensor

Pin Number	Pin	Description
1	OSC_IN	Oscillator input
2	OSC_OUT	Oscillator output
3	SDIO	Serial Port Data (input and output)
4	SCK	Serial Port Clock (Input)
5	LED_CNTL	Digital Shutter Signal Out
6	GND	System Ground
7	VDD	5V DC Input
8	REFA	Internal reference

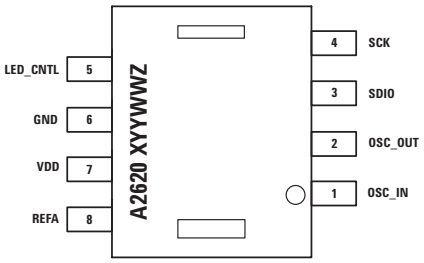
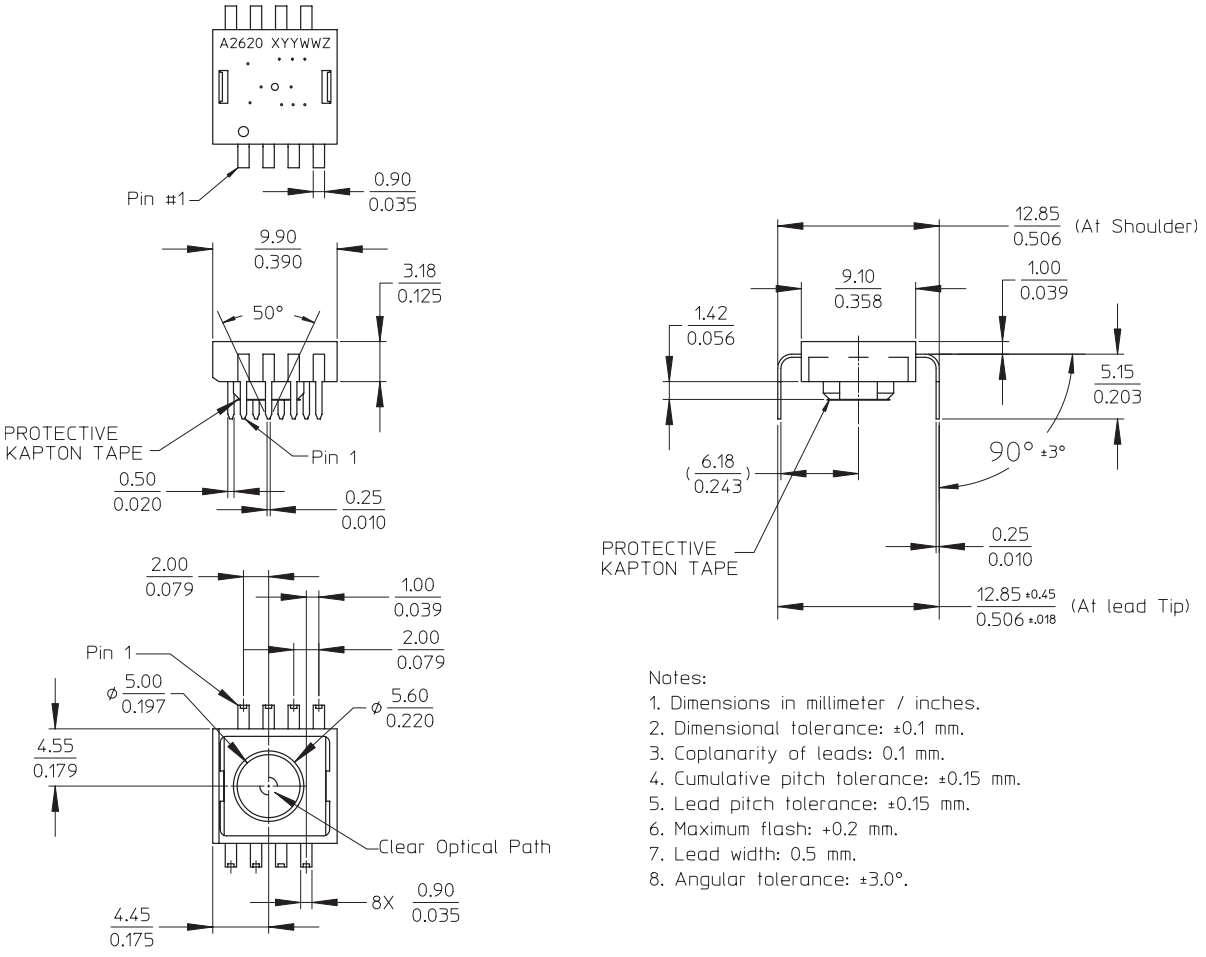


Figure 1. Mechanical drawing: top view.



Notes:
1. Dimensions in millimeter / inches.
2. Dimensional tolerance: ±0.1 mm.
3. Coplanarity of leads: 0.1 mm.
4. Cumulative pitch tolerance: ±0.15 mm.
5. Lead pitch tolerance: ±0.15 mm.
6. Maximum flash: +0.2 mm.
7. Lead width: 0.5 mm.
8. Angular tolerance: ±3.0°.

Figure 2. Package outline drawing.

CAUTION: It is advisable that normal static precautions should be taken in the handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Optical Mouse Sensor Assembly

NOTE: Pin 1 of optical mouse sensor should be inserted into the reference point of mechanical cutouts.

Figures 3 and 4 are shown with HDNS-2100, HDNS-2200 and HLMP-ED80-xx000.

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The components shown in Figure 5 interlock as they are mounted onto defined features on the base plate.

The ADNS-2620 sensor is designed for mounting on a through hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The HDNS-2100 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED. The lens also has a large round flange to provide a long creepage path for any ESD events that occur at the opening of the base plate.

The HDNS-2200 clip holds the LED in relation to the lens. The LED's leads must be formed first before inserting into the clip. Then, both LED and clip is loaded on the PCB. The clip interlocks the sensor to the lens, and through the lens to the alignment features on the base plate.

The HLMP-ED80-xx000 is recommended for illumination. If used with the bin table (as shown in Figure 8), sufficient illumination can be guaranteed.

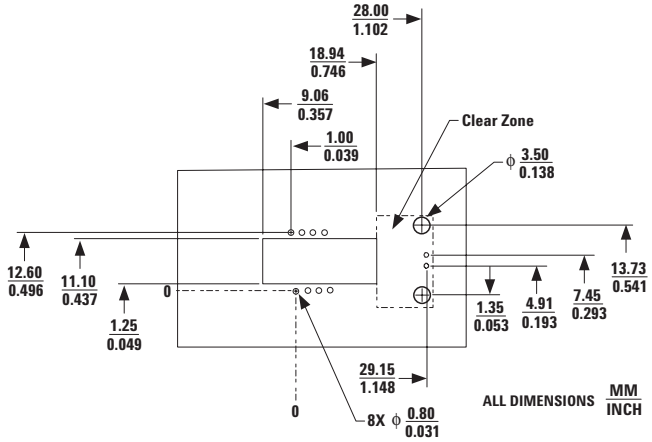


Figure 3. Recommended PCB mechanical cutouts and spacing.

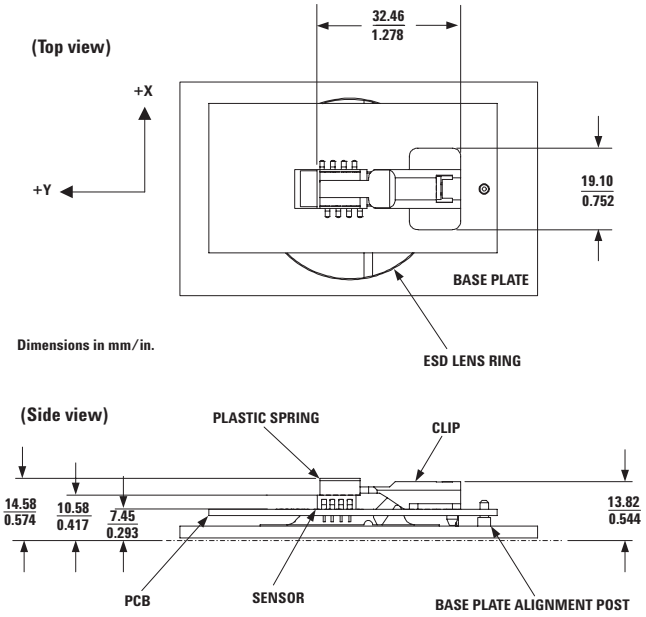


Figure 4. 2D assembly drawing of ADNS-2620 shown with the HLMP-ED80 (top and side view).

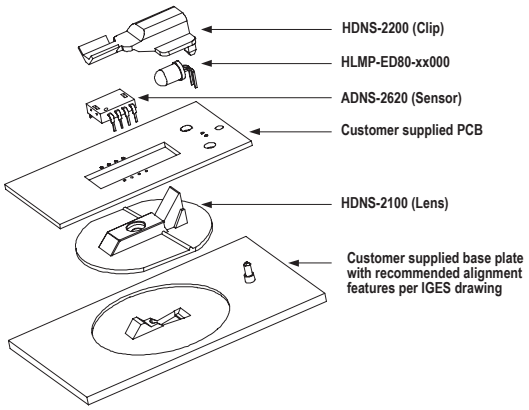


Figure 5. Exploded view drawing.

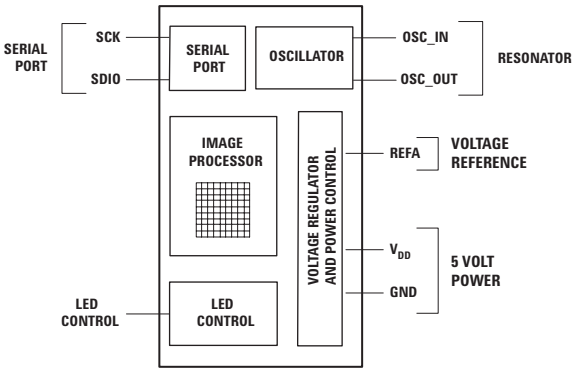


Figure 6. Block diagram of ADNS-2620 optical mouse sensor.

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB. Note: Pin 1 of the sensor should always be the reference point of mechanical cutouts.
2. Bend the LED leads 90° and then insert the LED into the assembly clip until the snap feature locks the LED base.
3. Insert the LED/clip assembly into PCB.
4. Wave solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact. The solder fixture is also used to set the reference height of the sensor to the PCB top during wave soldering (Note: DO NOT remove the kapton tape during wave soldering).
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. It is recommended not to place the PCB facing up during the entire mouse assembly process. The PCB should be held vertically for the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There MUST be a feature in the top case to press down onto the clip to ensure all components are interlocked to the correct vertical height.

Design Considerations for Improving ESD Performance

The flange on the lens has been designed to increase the creepage and clearance distance for electrostatic discharge. The table below shows typical values assuming base plate construction per the Avago supplied IGES file and HDNS-2100 lens flange.

Typical Distance	Millimeters
Creepage	16.0
Clearance	2.1

For improved ESD performance, the lens flange can be sealed (i.e. glued) to the base plate. Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

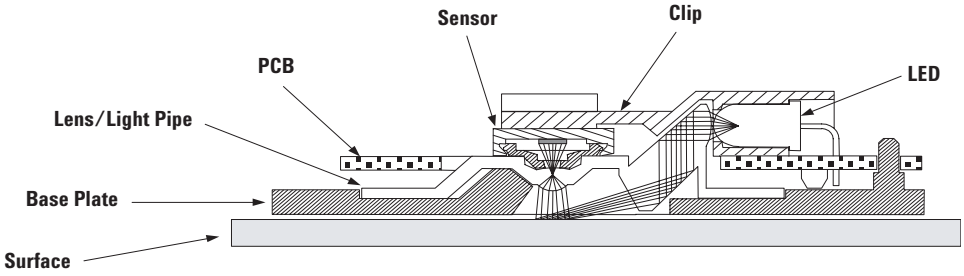


Figure 7. Sectional view of PCB assembly highlighting optical mouse components (optical mouse sensor, clip, lens, LED, PCB and base plate).

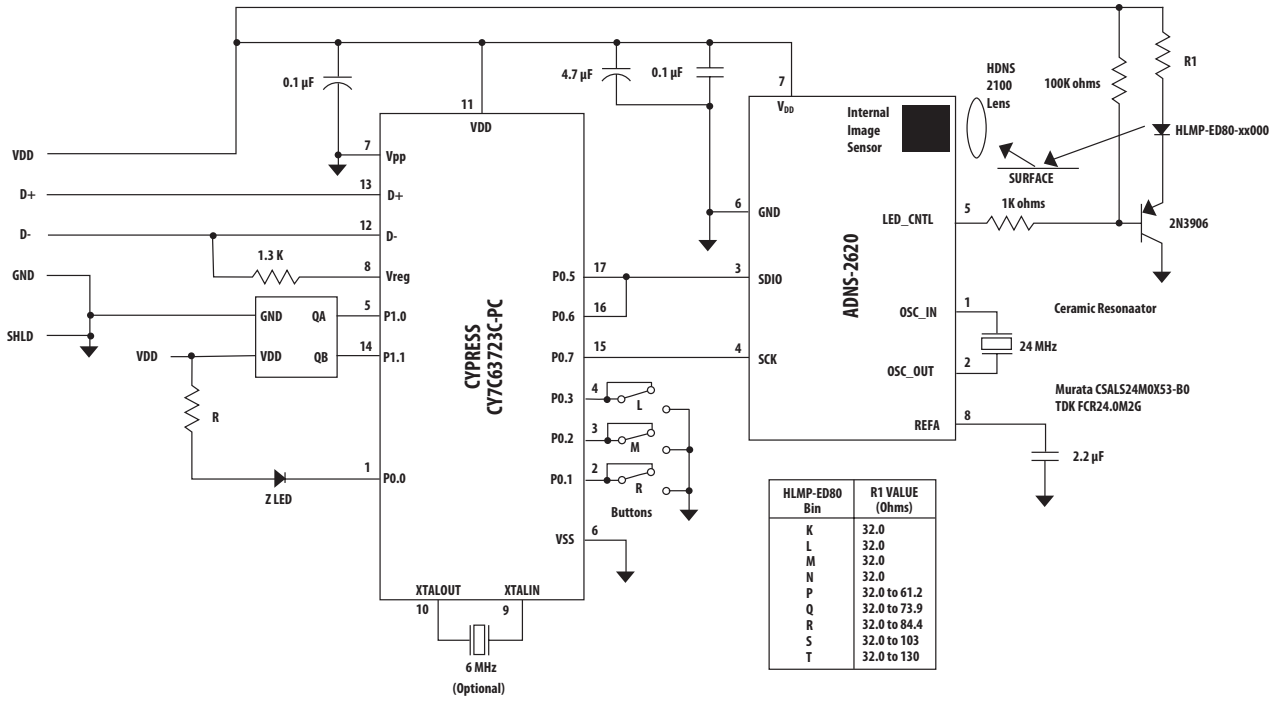


Figure 8. Circuit block diagram for a typical corded optical mouse using an Avago ADNS-2620 optical mouse sensor.

Notes on Bypass Capacitors

- Caps for pins 6,7 and 8 to ground *MUST* have trace lengths *LESS* than 5 mm.
- The 0.1 uF caps must be ceramic.
- Caps should have less than 5 nH of self inductance
- Caps should have less than 0.2 ohms ESR
- Surface mount parts are recommended

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with unshielded cable and following Avago recommendations.
- Passes EN61000-4-4/IEC801-4 EFTB tests when assembled into a mouse with shielded cable and following Avago recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15 kV when assembled into a mouse according to usage instructions above.
- For eye safety consideration, please refer to the technical report available on the web site at www.Avago.com/semiconductors.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temp			260	°C	For 10 seconds, 1.6 mm below seating plane
Supply Voltage	V_{DD}	-0.5	5.5	V	
ESD			2	KV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD}+0.5	V	SDIO, CLK, LED_CNTL
Input Voltage	V_{IN}	-0.5	3.6	V	OSC_IN, OSC_OUT, REFA

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	4.1	5.0	5.5	Volts	Register values retained for voltage transients below 4.10V but greater than 3.9V
Power Supply Rise Time	V_{RT}			100	ms	
Supply Noise	V_N			100	mV	Peak to peak within 0-100 MHz bandwidth
Clock Frequency	f_{CLK}	23.0	24.0	25.0	MHz	Set by ceramic resonator
Serial Port Clock Frequency	SCLK			f_{CLK}/12	MHz	
Resonator Impedance	X_{RES}			55	Ω	
Distance from Lens Reference Plane to Surface	Z	2.3	2.4	2.5	mm	Results in ±0.2 mm DOF (See Figure 9)
Speed	S	0		12	in/sec	@ frame rate = 1500 fps
Acceleration	A			0.25	g	@ frame rate = 1500 fps
Light Level onto IC	IRR_{INC}	80 100		25,000 30,000	mW/m^2	λ = 639 nm λ = 875 nm
SDIO Read Hold Time	t_{HOLD}	100			µs	Hold time for valid data (Refer to Figure 22)
SDIO Serial Write-write Time	t_{SWW}	100			µs	Time between two write commands (Refer to Figure 25)
SDIO Serial Write-read Time	t_{SWR}	100			µs	Time between write and read operation (Refer to Figure 26)
SDIO Serial Read-write Time	t_{SRW}	250			ns	Time between read and write operation (Refer to Figure 27)
SDIO Serial Read-read Time	t_{SRR}	250			ns	Time between two read commands (Refer to Figure 27)
Data Delay after PD deactivated	$t_{COMPUTE}$	3.1			ms	After $t_{COMPUTE}$, all registers contain data from first image after wakeup from Power-Down mode. Note that an additional 75 frames for AGC stabilization may be required if mouse movement occurred while Power Down. (Refer to Figure 10)
SDIO Write Setup Time	t_{SETUP}	60			ns	Data valid time before the rising of SCLK (Refer to Figure 20)
Frame Rate	FR		1500	2300	frames/s	See Frame_Period register section

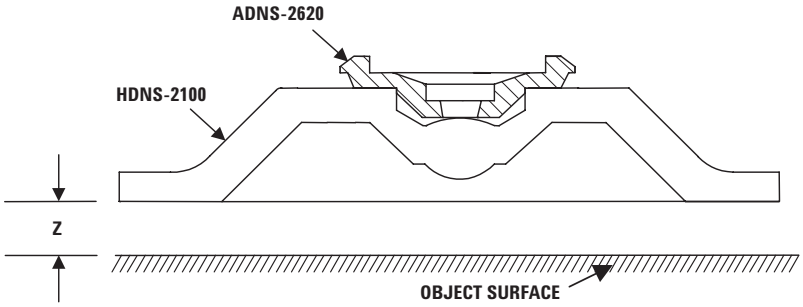


Figure 9. Distance from lens reference plane to surface.

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 5 V, 24 MHz, 1500 fps.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Power Down (PD)	t_{PD}	1.33			µs	32 clock cycle minimum after setting bit 6 in the Configuration register. (Refer to Figure 12)
Power Up after PD mode deactivated	t_{PUPD}			50	ms	From PD mode deactivation to accurate reports 610 µs + 75 frames (Refer to Figure 10)
Power Up from V_{DD} ↑	t_{PU}			40	ms	From V_{DD} to valid accurate reports 610 µs + 50 frames
Rise and Fall Times						
SDIO	t_r		30		ns	C_L = 30 pF (the rise time is between 10% to 90%)
	t_f		16		ns	C_L = 30 pF (the fall time is between 10% to 90%)
Serial Port Transaction Timer	t_{SPTT}		90		ms	Serial port will reset if current transaction is not complete within t_{SPTT} (Refer to Figure 29)
Transient Supply Current	I_{DDT}		20	37	mA	Max supply current during a V_{DD} ramp from 0 to 5.0V with > 500 µs rise time. Does not include charging current for bypass capacitors

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 5 V, 24 MHz, 1500 fps.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Current (mouse moving)	$I_{DD\ AVG}$		15	30	mA	
Supply Current (mouse not moving)	I_{DD}		12		mA	
Power Down Mode Current	I_{DDPD}		170	230	µA	
SCK pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input Capacitance	C_{IN}			10	pF	
Input Resistance	R_{IN}	1			MΩ	
SDIO pin						V_{DD}=4 V, Load = 50 pF, 80n s rise & fall
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.5	V	
Output High Voltage	V_{OH}	0.8 * V_{DD}			V	
Drive Low Current	I_L	2.0			mA	
Drive High Current	I_H	2.0			mA	
Input Capacitance	C_{IN}			10	pF	
Input Resistance	R_{IN}	1			MΩ	
LED_CNTL pin						
Output Low Voltage	V_{OL}			0.1	V	
Output High Voltage	V_{OH}	0.8 * V_{DD}			V	
Drive Low Current	I_L	250			µA	
Drive High Current	I_H	250			µA	
OSC_IN						
Input Resistance	R_{IN}		500		kΩ	
Input Capacitance	C_{IN}		15		pF	
Input High Voltage	V_{IH}	2.2			V	External clock source
Input Low Voltage	V_{IL}			0.8	V	External clock source

PD Pin Timing

Note: All timing circuits shown, from Figure 10 onwards, are based on the 24 MHz resonator frequency.

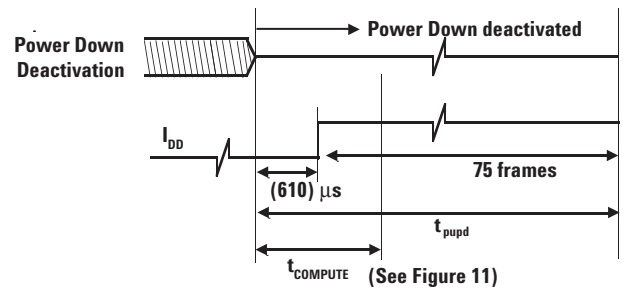


Figure 10. Power up timing mode.

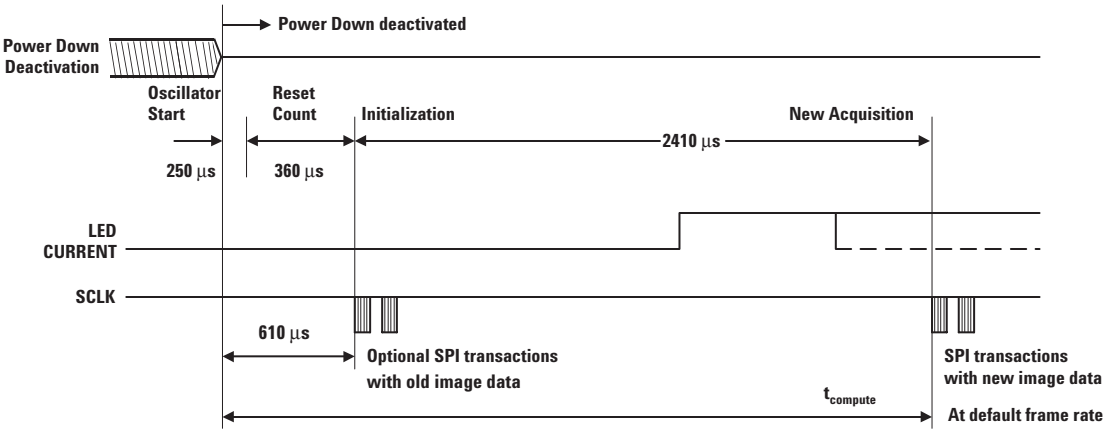


Figure 11. Details of wake-up timing after PD.

Power-down Mode (PD) and Timing

ADNS-2620 can be placed in a power-down mode by setting bit 6 in the configuration register via a serial I/O port write operation. Note that while writing a "1" to bit 6 of the configuration register, all other bits must be written with their original value in order to keep the current configuration. After setting the configuration register, wait at least 32 system clock cycles. To get the chip out of the power-down mode, clear bit 6 in the configuration register via a serial I/O port write operation. (CAUTION! In power-down mode, the SPI timeout (t_{SPTT}) will not function. Therefore, no partial SPI command should be sent. Otherwise, the sensor may go into a hang-up state). While the sensor is in power-down mode, only the bit 6 data will be written to the configuration register. Writing the other configuration register values will not have any effect. For an accurate report after power-up, wait for a total period of 50 ms before the microcontroller is able to issue any write/read operation to the ADNS-2620. The sensor register settings, prior to power-down mode, will remain during power-down mode.

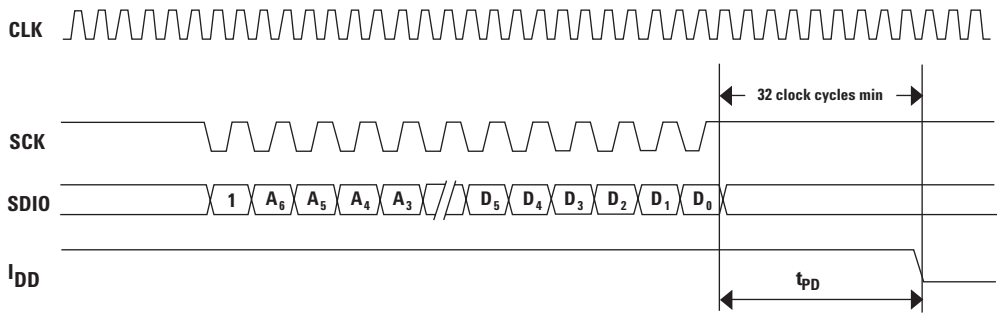


Figure 12. Power-down timing.

The address of the configuration register is 1000000.

Assume that the original content of the configuration register is 0x00.

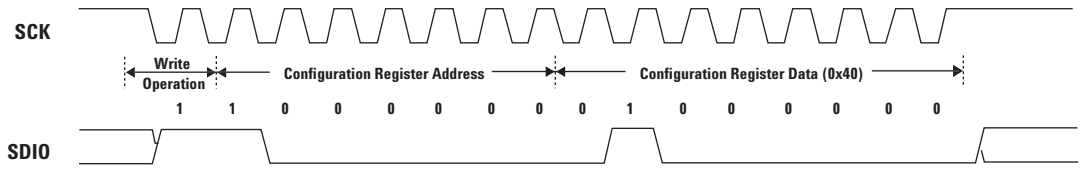


Figure 13. Power-down configuration register writing operation.

Setting the power down bit simply sets the analog circuitry into a no current state.

Note: LED_CNTL, and SDIO will be tri-stated during power down mode.

Typical Performance Characteristics

Performance characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 5 V, 24 MHz, 1500 fps.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Path Error (Deviation)	P_{Error}		0.5		%	Path Error (Deviation) is the error from the ideal cursor path. It is expressed as a percentage of total travel and is measured over standard surfaces.

The following graphs (Figures 14-18) are the typical performance of the ADNS-2620 sensor, assembled as shown in the 2D assembly drawing with the HDNS-2100 Lens/Prism, the HDNS-2200 clip, and the HLMP-ED80-xx000 (See Figure 4).

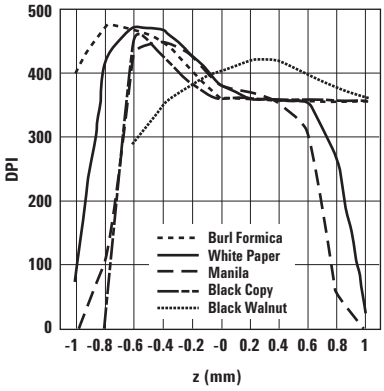


Figure 14. Typical Resolution vs. Z (comparative surfaces)

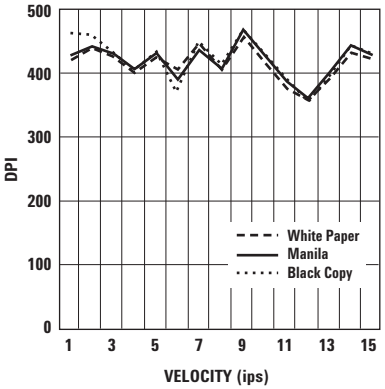


Figure 15. Typical Resolution vs. Velocity @ 1500 fps.

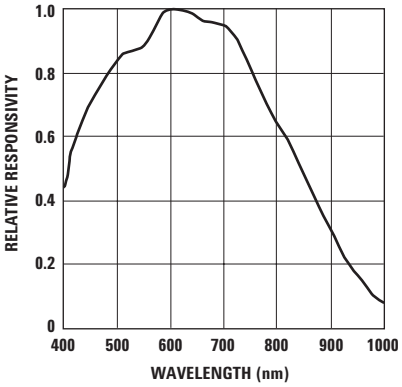


Figure 16. Wavelength Responsivity[1].

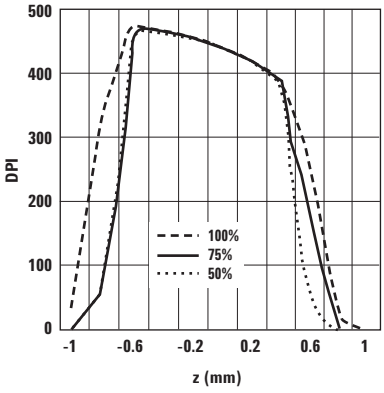


Figure 17. Typical Resolution vs. Height at different LED currents on manila.

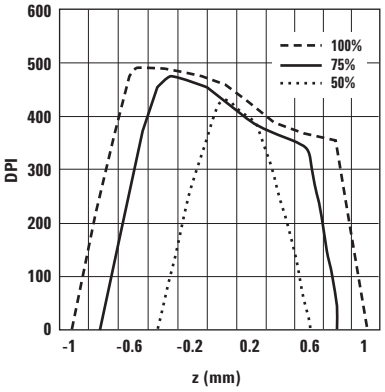


Figure 18. Typical Resolution vs. Height at different LED currents on black.

Notes:
1. The ADNS-2620 is designed for optimal performance when used with the HLMP-ED80-xx000 (red LED 639 nm). For use with other LED colors (i.e., blue, green), please consult factory. When using alternate LEDs, there may also be performance degradation and additional eye safety considerations.
2. Z = Distance from Lens Reference plane to Surface.
3. DOF = Depth of Field.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-2620, and also to read out the motion information.

The port is a two wire, half duplex port. The host microcontroller always initiates communication; the ADNS-2620 never initiates data transfers.

SCK: The serial port clock. It is always generated by the master (the microcontroller).

SDIO: The data line.

Write Operation

Write operations, where data is going from the microcontroller to the ADNS-2620, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The transfer is synchronized by **SCK**. The microcontroller changes **SDIO** on falling edges of **SCK**. The ADNS-2620 reads **SDIO** on rising edges of **SCK.**

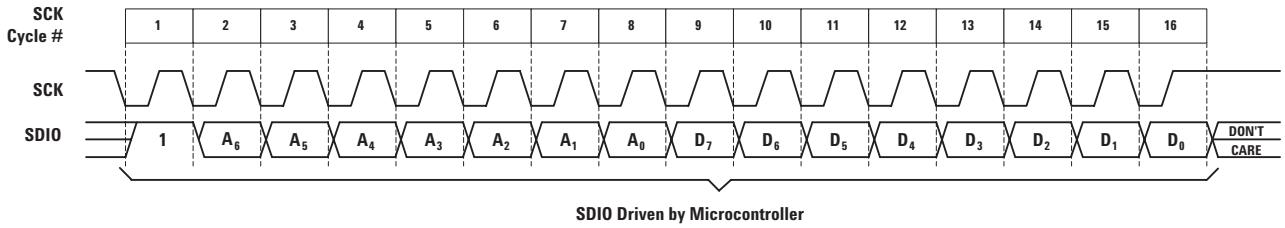


Figure 19. Write operation.

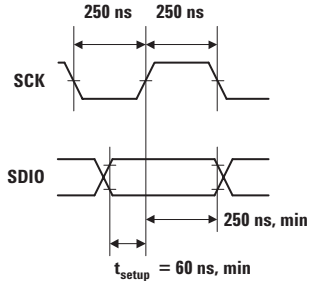


Figure 20. SDIO setup and hold times SCK pulse width.

Read Operation

A read operation, meaning data that is going from the ADNS-2620 to the microcontroller, is always initiated by the microcontroller and consists of two bytes. The first byte that contains the address is written by the microcontroller and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-2620. The transfer is synchronized by **SCK**. **SDIO** is changed on falling edges of **SCK** and read on every rising edge of **SCK**. The microcontroller must go to a High-Z state after the last address data bit. The ADNS-2620 will go to the High-Z state after the last data bit. Another thing to note during a read operation is that SCK needs to be delayed after the last address data bit to ensure that the ADNS-2620 has at least 100 µs to prepare the requested data. This is shown in the timing diagrams below (See Figures 21 to 23).

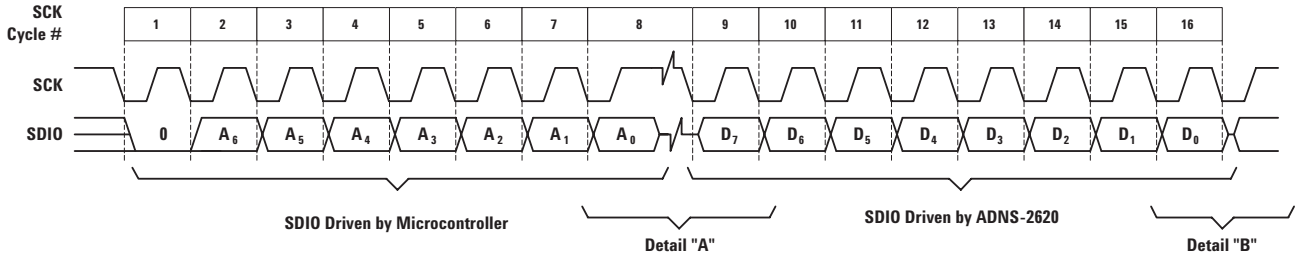


Figure 21. Read operation.

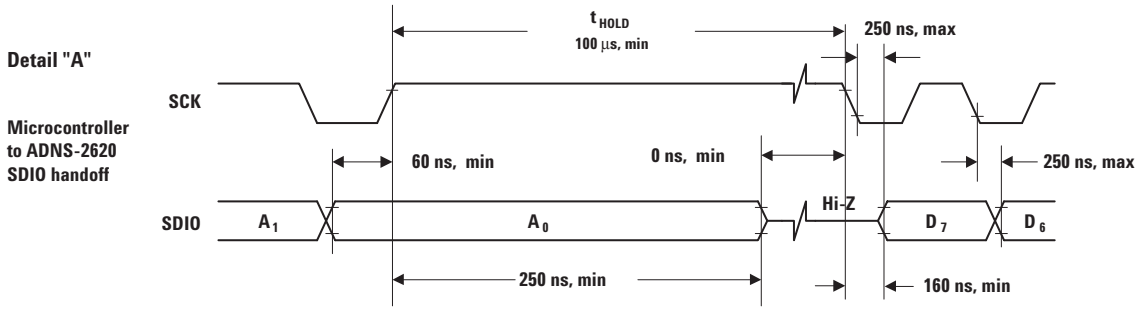


Figure 22. Microcontroller to ADNS-2620 SDIO handoff.

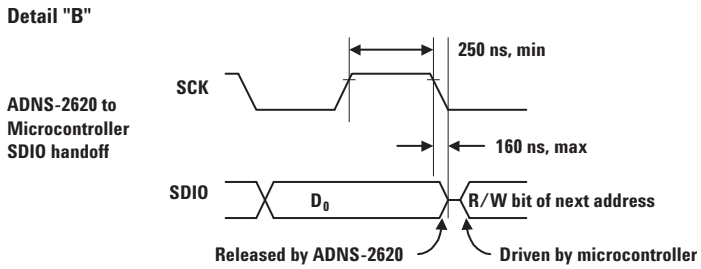


Figure 23. ADNS-2620 to microcontroller SDIO handoff.

NOTE:
The 250 ns high state of SCK is the minimum data hold time of the ADNS-2620. Since the falling edge of SCK is actually the start of the next read or write command, the ADNS-2620 will hold the state of D_0 on the SDIO line until the falling edge of SCK. In both write and read operations, SCK is driven by the microcontroller.

Forcing the SDIO Line to the Hi-Z State

There are times when the SDIO line from the ADNS-2620 should be in the Hi-Z state. For example, if the microprocessor has completed a write to the ADNS-2620, the SDIO line will go into a Hi-Z state, because the SDIO pin was configured as an input. However, if the last operation from the microprocessor was a read, the ADNS-2620 will hold the D0 state on SDIO until a falling edge of SCK.

To place the SDIO pin into a Hi-Z state, activate the power-down mode by writing to the configuration register. Then, the powerdown mode can stay activated, with the ADNS-2620 in the shutdown state, or the power-down mode can be deactivated, returning the ADNS-2620 to normal operation. In both conditions, the SDIO line will go into the Hi-Z state.

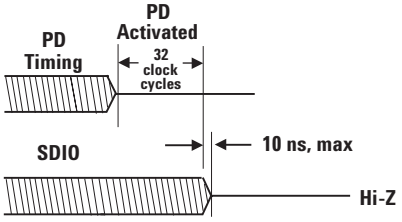


Figure 24. SDIO Hi-z state and timing.

Another method to put the SDIO line into the Hi-Z state, while maintaining the ADNS-2620 at normal mode, is to write any data to an invalid address such as 0x00 to address 0x77. The SDIO line will go into the Hi-Z state after the write operations.

Required Timing between Read and Write Commands (tsxx)

There are minimum timing requirements between read and write commands on the serial port.

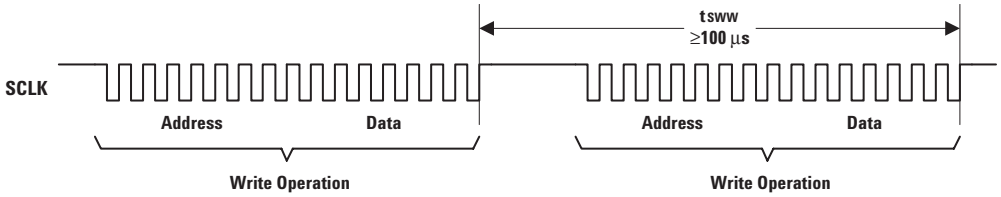


Figure 25. Timing between two write commands.

If the rising edge of the SCK for the last data bit of the second write command occurs before the 100 µs required delay, then the first write command may not complete correctly.

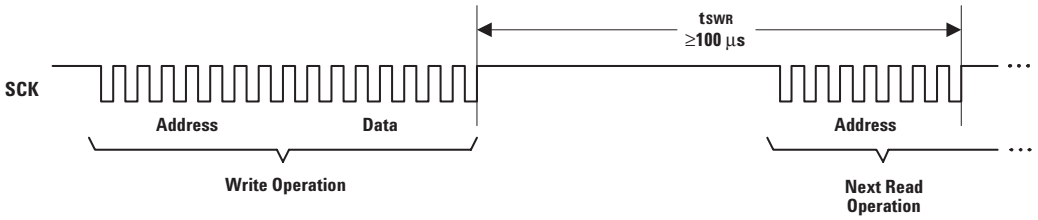


Figure 26. Timing between write and read commands.

If the rising edge of SCK for the last address bit of the read command occurs before the 100 µs required delay, then the write command may not complete correctly.

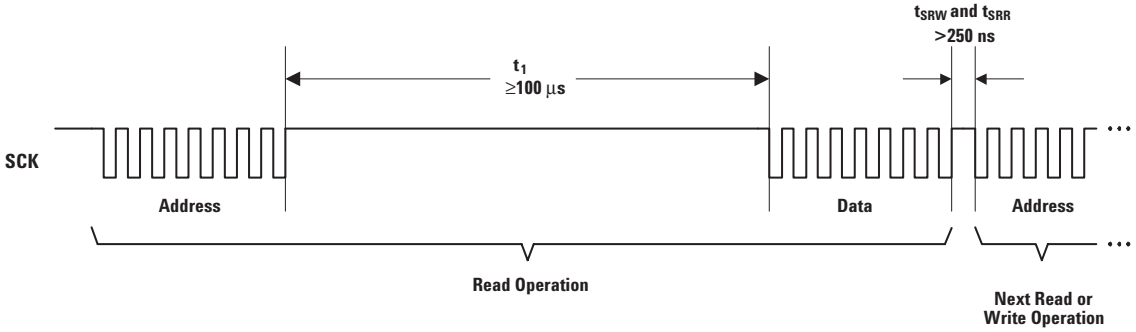


Figure 27. Timing between read and either write or subsequent read commands.

The falling edge of SCK for the first address bit of either the read or write command must be at least 250 ns after the last SCK rising edge of the last data bit of the previous read operation.

Error Detection and Recovery

1. The ADNS-2620 and the microcontroller might get out of synchronization due to ESD events, power supply droops or microcontroller firmware flaws.
2. The ADNS-2620 has a transaction timer for the serial port. If the sixteenth SCK rising edge is spaced more than approximately 90 milliseconds from the first SCK edge of the current transaction, the serial port will reset.
3. Invalid addresses:
   - Writing to an invalid address will have no effect. Reading from an invalid address will return all zeros.
4. Collision detection on SDIO
   - The only time that the ADNS-2620 drives the SDIO line is during a READ operation. To avoid data collisions, the microcontroller should relinquish SDIO before the falling edge of SCK after the last address bit. Then the ADNS-2620 begins to drive SDIO after the next rising edge of SCK. Next, the ADNS-2620 relinquishes SDIO within 160 ns of the falling SCK edge after the last data bit. The microcontroller can begin driving SDIO any time after that. In order to maintain low power consumption in normal operation or when the PD bit is set high, the microcontroller should not leave SDIO floating until the next transmission (although that will not cause any communication difficulties).
5. In case of synchronization failure, both the ADNS-2620 and the microcontroller may drive SDIO. The ADNS-2620 can withstand 30 mA of short circuit current and will withstand infinite duration short circuit conditions.
6. The microcontroller can verify a successful write operation by issuing a read command to the same address and comparing the written data to the read data.
7. The microcontroller can verify the synchronization of the serial port by periodically reading the product ID from status register (Address: 0x41).

Notes on Power-up and the Serial Port

The sequence in which V_{DD}, SCK and SDIO are set during powerup can affect the operation of the serial port. The diagram below shows what can happen shortly after powerup when the microprocessor tries to read data from the serial port.

This diagram shows the V_{DD} rising to valid levels, at some point the microcontroller starts its program, sets the SCK and SDIO lines to be outputs, and sets them high. Then, the microcontroller waits to ensure the ADNS-2620 has powered up and is ready to communicate. The microprocessor then tries to read from location 0x41, Status register, and is expecting a value of 0x0b010XXXXX. If it receives this value, then it knows that the communication to the ADNS-2620 is operational.

The problem occurs if the ADNS-2620 powers up before the microprocessor sets the SCK and SDIO lines to be outputs and high. The ADNS-2620 sees the raising of the SCK as a valid rising edge, and clocks in the state of the SDIO as the first bit of the address (sets either a read or a write depending upon the state).

In the case of a SDIO low, a read operation will start. When the microprocessor actually begins to send the address, the ADNS-2620 already has the first bit of an address. When the seventh bit is sent by the microprocessor, the ADNS-2620 has a valid address, and drives the SDIO line high within 250 ns (see detail "A" in Figure 19 and Figure 20). This results in a bus fight for SDIO. Since the address is wrong, the data sent back will be incorrect.

In the case of a SDIO high, a write operation will start. The address and data will be out of synchronization, causing the wrong data written to the wrong address.

Solution

One way to solve the problem is by waiting for the serial port timer to time out.

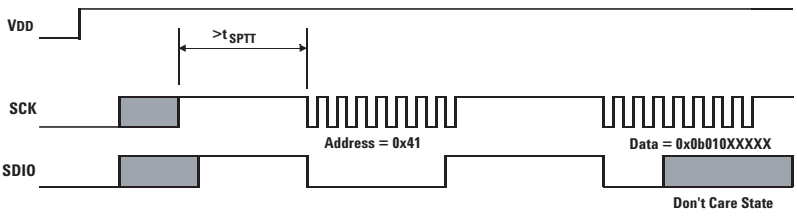


Figure 28. Power-up serial port sequence.

Serial Port Timer Timeout

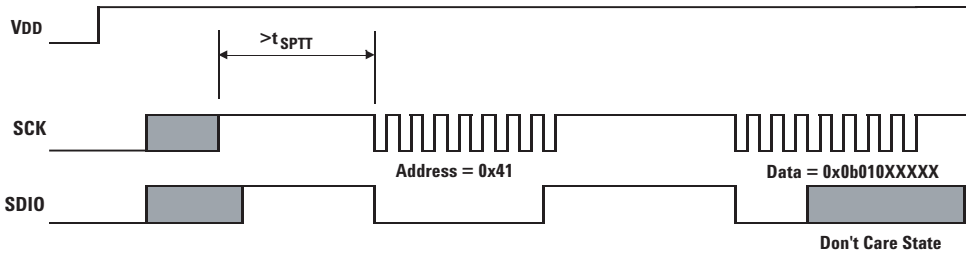


Figure 29. Power-up serial port timer sequence.

If the microprocessor waits at least t_{SPTT} from V_{DD} valid, it will ensure that the ADNS-2620 has powered up and the timer has timed out. This assumes that the microprocessor and the ADNS-2620 share the same power supply. If not, then the microprocessor must wait for t_{SPTT} from ADNS-2620 V_{DD} valid. Then when the SCK toggles for the address, the ADNS-2620 will be in sync with the microprocessor.

Resync Note

If the microprocessor and the ADNS-2620 get out of sync, then the data either written or read from the registers will be incorrect. An easy way to solve this is to use watchdog timer timeout sequence to resync the parts after an incorrect read.

Power-up

ADNS-2620 has an on-chip internal power-up reset (POR) circuit, which will reset the chip when VDD reaches the valid value for the chip to function.

Soft Reset

ADNS-2620 may also be given the reset command at any time via the serial I/O port. The timing and transactions are the same as those just specified for the power-up mode in the previous section.

The proper way to perform soft reset on ADNS-2620 is:

1. The microcontroller starts the transaction by sending a write operation containing the address of the configuration register and the data value of 0x80. Since the reset bit is set, ADNS-2620 will reset and any other bits written into the configuration register at this time is properly written into the Configuration Register. After the chip has been reset, very quickly, ADNS-2620 will clear the reset bit so there is no need for the microcontroller to re-write the Configuration Register to reset it.
2. The digital section is now ready to go. It takes 3 frames for the analog section to settle.

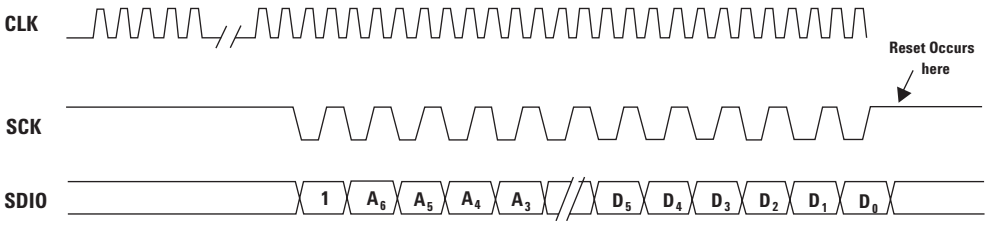


Figure 30. ADNS-2620 soft reset sequence timing.

Soft reset will occur when writing 0x80 to the configuration register.

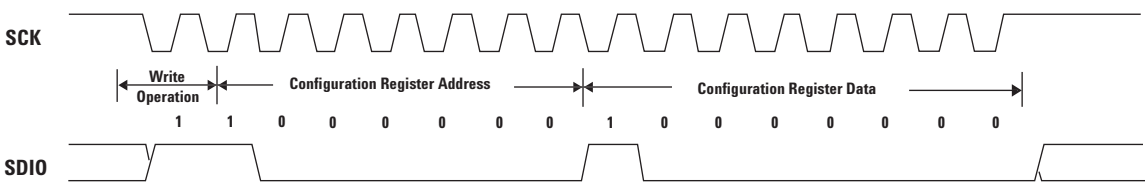


Figure 31. Soft reset configuration register writing operation.

Programming Guide

Registers

The ADNS-2620 can be programmed through registers, via the serial port, and configuration and motion data can be read from these registers.

Register	Address	Notes
Configuration	0x40	Reset, Power Down, Forced Awake, etc
Status	0x41	Product ID, Mouse state of Asleep or Awake
Delta_Y	0x42	Y Movement
Delta_X	0x43	X Movement
SQUAL	0x44	Measure of the number of features visible by the sensor
Maximum_Pixel	0x45	
Minimum_Pixel	0x46	
Pixel_Sum	0x47	
Pixel Data	0x48	Actual picture of surface
Shutter_Upper	0x49	
Shutter_Lower	0x4A	
Frame Period	0x4B	

Configuration **Address: 0x40**
Access: Read/Write **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

Data Type**:** Bit field

USAGE: The Configuration register allows the user to change the configuration of the sensor. Shown below are the bits, their default values, and optional values.

Field Name	Description
C_7	Reset **0 = No effect** 1 = Reset the part
C_6	Power down **0 = Normal operation** 1 = power down all analog circuitry
C_5	LED Shutter Mode **0= Shutter mode off (LED always on even if no motion up to 1 sec)** 1= Shutter mode on (LED only on when electronic shutter is open)
$C_{4-}C_1$	Reserved
C_0	Forced Awake Mode **0 = Normal, fall asleep after one second of no movement (1500 frames/s)** 1 = Always awake

Status **Address: 0x41**
Access: Read **Reset Value: 0x41**

Bit	7	6	5	4	3	2	1	0
Field	ID_2	ID_1	ID_0	Reserved	Reserved	Reserved	Reserved	Awake

Data Type: Bit Field

USAGE: Status information and type of mouse sensor, current state of the mouse.

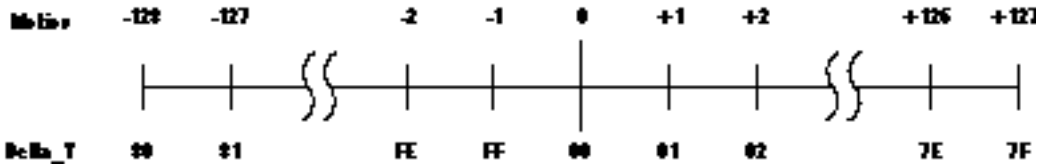
Field Name	Description
$ID_{2-}ID_0$	Product ID (010 for ADNS-2620)
Reserved	Reserved for future
Awake	Mouse State **0 = Asleep** 1 = Awake

Delta_Y **Address: 0x42**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counted since last report. Absolute value is determined by resolution. Reading clears the register.

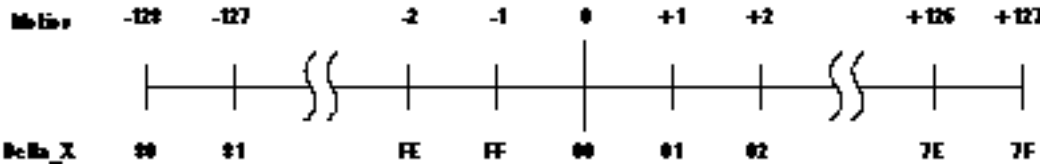


Delta_X **Address: 0x43**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counted since last report. Absolute value is determined by resolution. Reading clears the register



SQUAL **Address: 0x44**
Access: Read **Reset Value: 0x00**

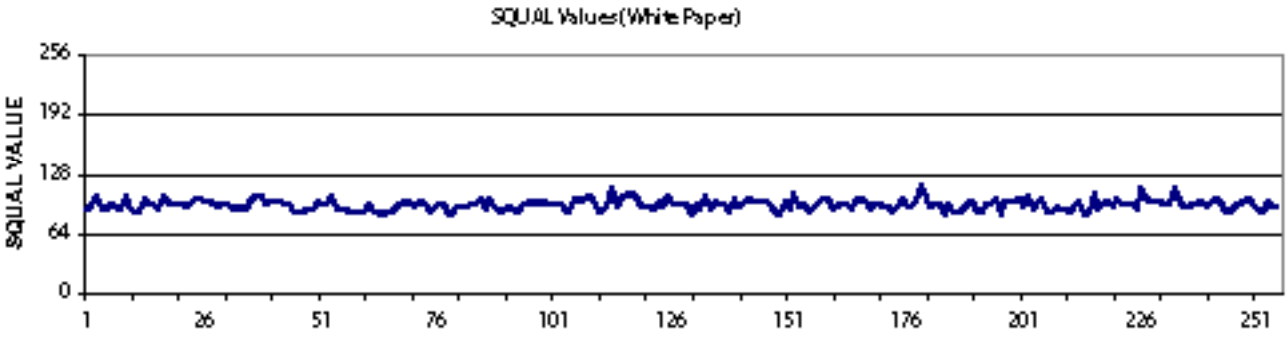
Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8 bits of a 9-bit integer.

USAGE: SQUAL (Surface QUALity) is a measure of the number of features visible by the sensor in the current frame.

Number of Features = SQUAL Register Value x 2.

The maximum value is 255. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero when there is no surface below the sensor.



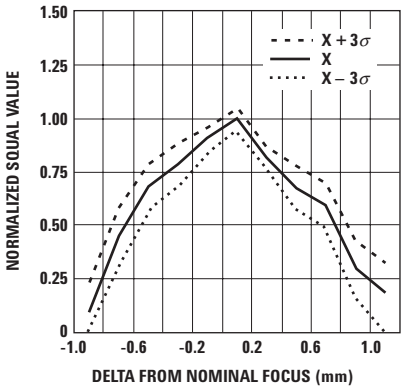


Figure 32. Typical Mean SQUAL vs. z (white paper).

The focus point is important and could affect the SQUAL value. Figure 32 shows another setup with various z-heights. This graph clearly shows that the SQUAL value is dependent on focus distance.

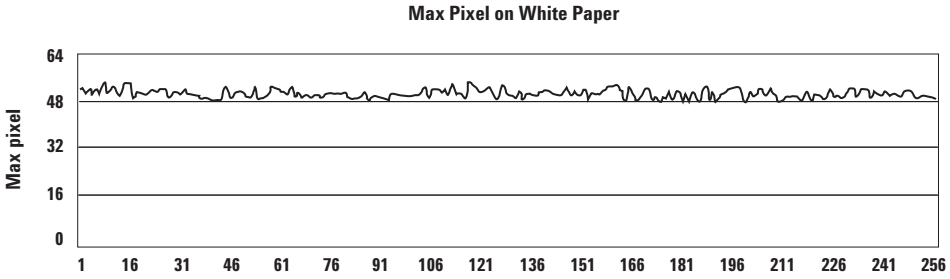
Note: The data is obtained by getting multiple readings over different heights.

Maximum_Pixel **Address: 0x45**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	0	0	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Six bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 63. The maximum pixel value may vary from frame to frame. Shown below is a graph of 250 sequentially acquired maximum pixel values, while the sensor was moved slowly over white paper.

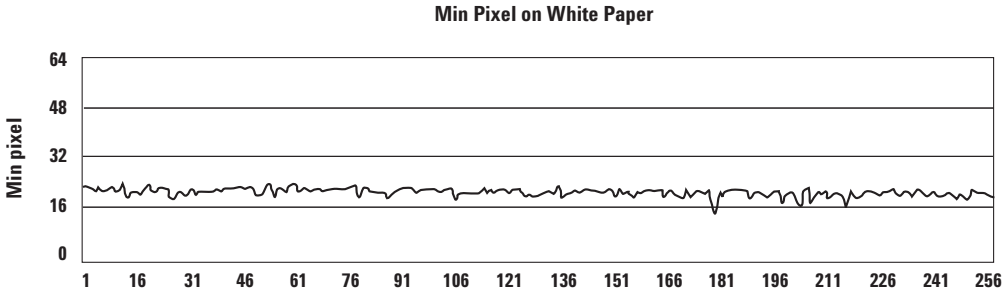


Minimum_Pixel **Address: 0x46**
Access: Read **Reset Value: 0x3f**

Bit	7	6	5	4	3	2	1	0
Field	0	0	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Six bit number.

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 63. The minimum pixel value may vary from frame to frame.



Pixel_Sum **Address: 0x47**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	PS_7	PS_6	PS_5	PS_4	PS_3	PS_2	PS_1	PS_0

Data Type: Upper 8 bits of a 15-bit unsigned integer.

USAGE: This register is used to find the average pixel value. It reports the upper 8 bits of a 15-bit unsigned integer, which sums all 324 pixels in the current frame. It may be described as the full sum divided by 128. The formula to calculate the average pixel value is as below:

Average Pixel = Register Value x 128 / 324

= Pixel_Sum x 0.395

The maximum register value is 159 (63 x 324 / 128 truncated to an integer). The minimum is 0. The pixel sum value may vary from frame to frame.

Pixel Data **Address: 0x48**
Access: Read/Write **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	SOF	Data_Valid	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

Data Type: Two status bits, six bit pixel data.

USAGE: Digital Pixel data. Minimum value = 0, maximum value = 63. Any writes to this register resets the pixel hardware so that the next read from the Pixel Data register will read pixel #1 and the StartOfFrame bit will be set. Subsequent reads will auto increment the pixel number.

To dump a complete image, set the LED to forced awake mode, write anything to this register, then read 324 times where the DataValid bit is set. On the 325th read, the StartOfFrame bit will be set indicating that we have completed one frame of pixels and are starting back at pixel 1.

It takes at least 324 frames to complete an image as we can only read 1 pixel per frame.

The pixel hardware is armed with any read or write to the Pixel Data register and will output pixel data from the next available frame. So, if you were to write the Pixel Data register, wait 5 seconds then read the Pixel Data register; the reported pixel data was from 5 seconds ago.

Field Name	Description
SOF	Start of Frame **0 = Not start of frame** 1 = Current pixel is number 1, start of frame
Data_Valid	There is valid data in the frame grabber
PD_5 – PD_0	Six bit pixel data

Pixel Map (sensor is facing down, looking through the sensor at the surface)

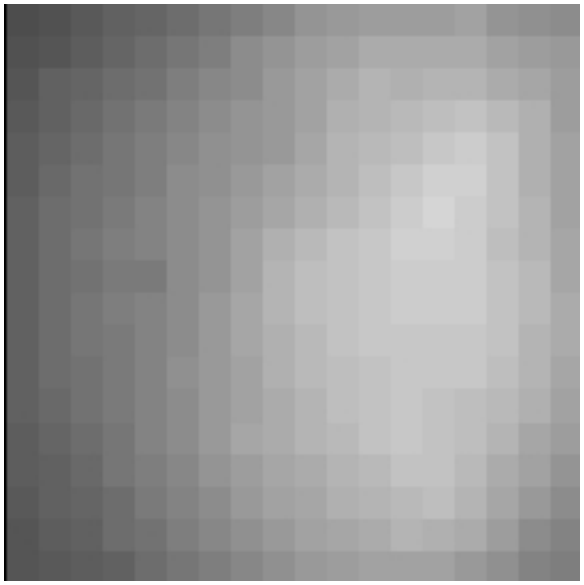
Last Pixel

18	36	54	72	90	108	126	144	162	180	198	216	234	252	270	288	306	324
17	35	53	71	89	107	125	143	161	179	197	215	233	251	269	287	305	323
16	34	52	70	88	106	124	142	160	178	196	214	232	250	268	286	304	322
15	33	51	69	87	105	123	141	159	177	195	213	231	249	267	285	303	321
14	32	50	68	86	104	122	140	158	176	194	212	230	248	266	284	302	320
13	31	49	67	85	103	121	139	157	175	193	211	229	247	265	283	301	319
12	30	48	66	84	102	120	138	156	174	192	210	228	246	264	282	300	318
11	29	47	65	83	101	119	137	155	173	191	209	227	245	263	281	299	317
10	28	46	64	82	100	118	136	154	172	190	208	226	244	262	280	298	316
9	27	45	63	81	99	117	135	153	171	189	207	225	243	261	279	297	315
8	26	44	62	80	98	116	134	152	170	188	206	224	242	260	278	296	314
7	25	43	61	79	97	115	133	151	169	187	205	223	241	259	277	295	313
6	24	42	60	78	96	114	132	150	168	186	204	222	240	258	276	294	312
5	23	41	59	77	95	113	131	149	167	185	203	221	239	257	275	293	311
4	22	40	58	76	94	112	130	148	166	184	202	220	238	256	274	292	310
3	21	39	57	75	93	111	129	147	165	183	201	219	237	255	273	291	309
2	20	38	56	74	92	110	128	146	164	182	200	218	236	254	272	290	308
1	19	37	55	73	91	109	127	145	163	181	199	217	235	253	271	289	307

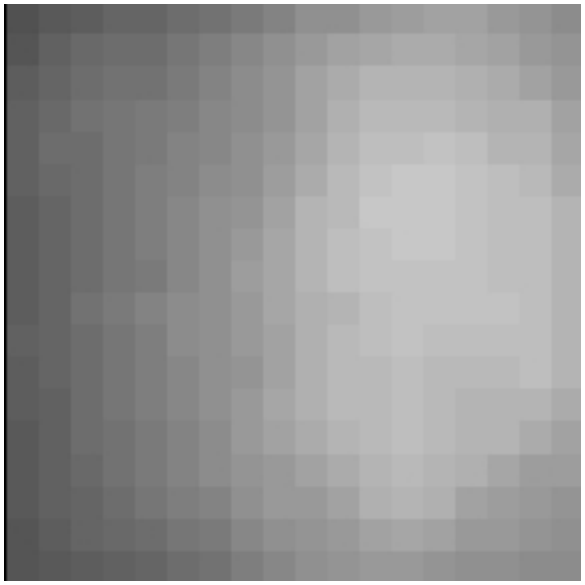
First Pixel

Pixel Dump Pictures

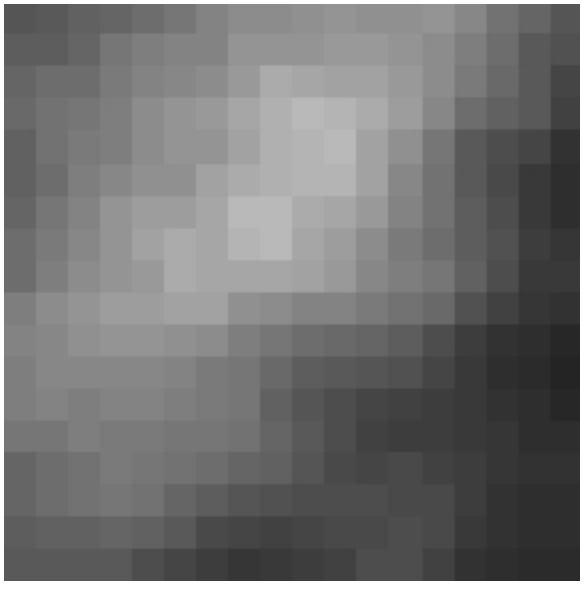
The following images are the output of the Pixel Data command. The data ranges from 0 for complete black, to 63 for complete white. An internal AGC circuit adjusts the shutter value to keep the brightest feature (max pixel) in the mid 50's.



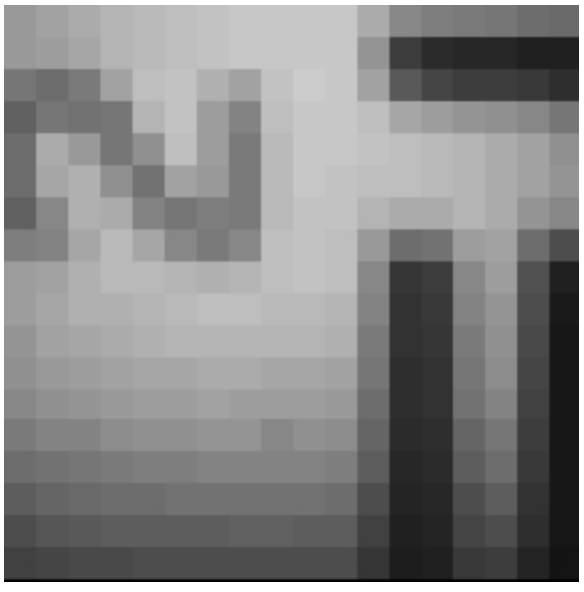
(a) White Paper



(b) Manila Folder



(c) Burl Formica



(d) USAF Test Chart

Shutter_Upper **Address: 0x49**
Access: Read **Reset Value: 0x01**

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower **Address: 0x4A**
Access: Read **Reset Value: 0x00**

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type: Sixteen bit word.

USAGE: Units are clock cycles; default value is $0x0100_{HEX}$. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The sensor adjusts the shutter to keep the average and maximum pixel values within normal operating ranges. The shutter value may vary with every frame. Each time the shutter changes, it changes by ±1/16 of the current value.

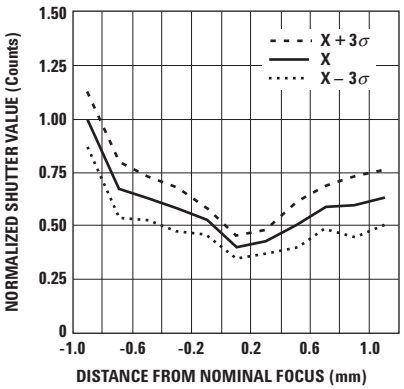


Figure 33. Typical Mean Shutter vs. z (white paper).

Note:
This graph is obtained by getting multiple readings over different heights.

The maximum value of the shutter is dependent upon the clock frequency. The formula for the maximum shutter value is:

$$\text{Max shutter value} = \frac{\text{clock freq}}{\text{Frame Rate}} - 3476$$

For a clock frequency of 24 MHz, the following table shows the maximum shutter value. 1 clock cycle is 41.67 nsec.

Frames/second	Max Shutter		Shutter		
	Decimal	Hex	Upper	Lower	
3000	4524	0x11AC	11	AC	
1512	12397	0x306D	30	6D	<-- Default Max Shutter
369	61564	0xF07C	F0	7C	

Frame_Period **Address: 0x4b**
Access: Read/Write **Reset Value: 0xc2**

Bit	7	6	5	4	3	2	1	0
Field	FP_7	FP_6	FP_5	FP_4	FP_3	FP_2	FP_1	FP_0

Data Type: Eight bit 2's complement number that represents the upper 8 bits of a 16 bit counter.

USAGE: The frame period counter counts up until it overflows. Units are clock cycles. The formula is:

$$\frac{\text{Clock Rate}}{\text{Frame Rate}} = \text{Counts (decimal)} \longrightarrow \text{Counts (hex)} \longrightarrow \text{Counts (2's complement hex)}$$

Frame Rate (frames/sec)	Clocks/Frame Decimal	Clocks/Frame (2's complement hex)	
369	65024	02	<-- Maximum Frame Time
1512	15872	C2	<-- Nominal Frame Time
3000	8000	E0	

Note:

To optimize tracking performance on dark surfaces, it is recommended that an adaptive frame rate based on shutter value be implemented for frame rates greater than 1500.

Changing the frame rate results in changes in the maximum speed, acceleration limits, and dark surface performance.

Ordering Information

Specify part number as follows:

ADNS-2620 = 8-pin staggered dual inline package (DIP), 40 per tube.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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